

**FIG.1**  
**PRIOR ART**

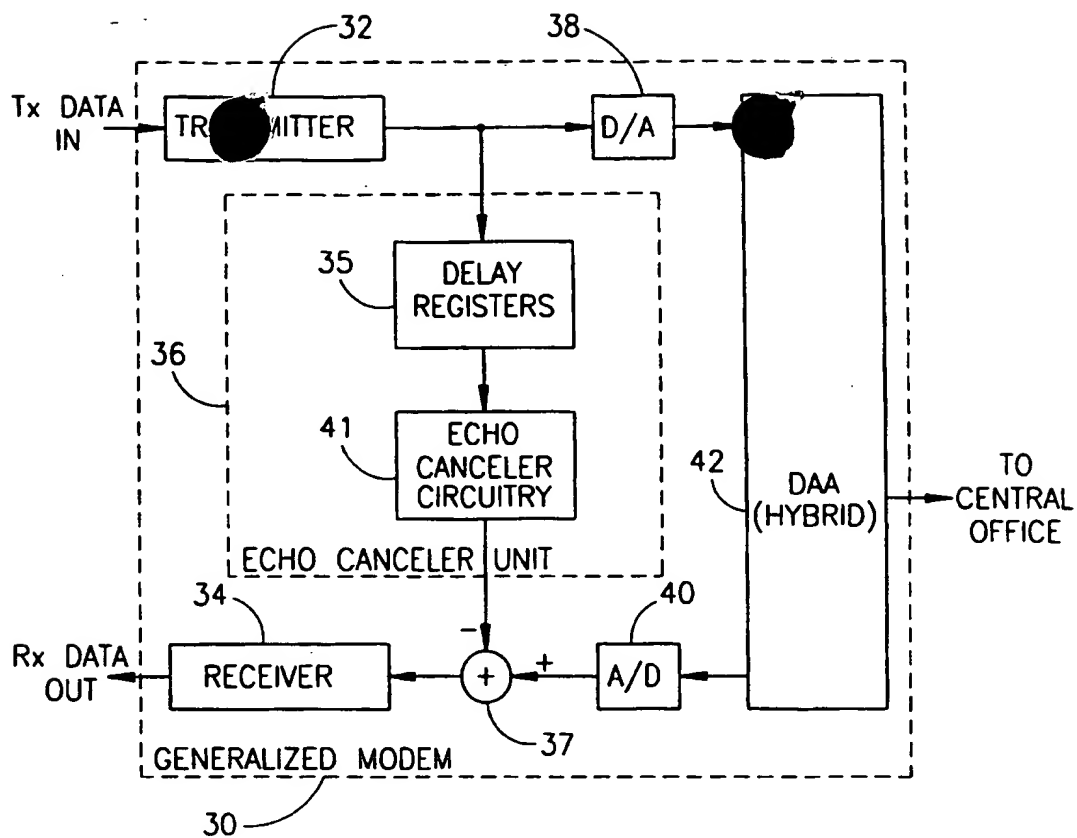
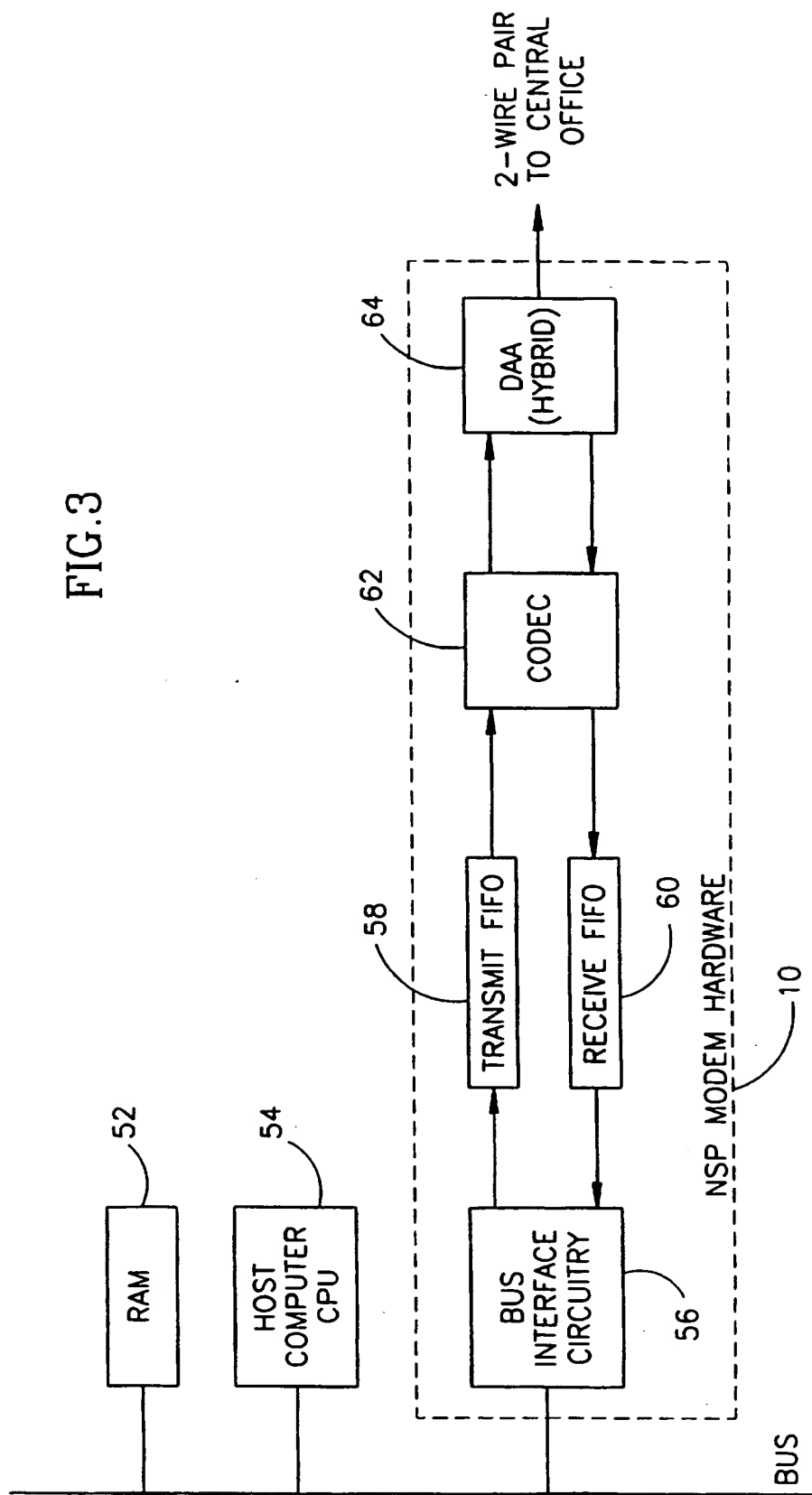


FIG.2

FIG. 3



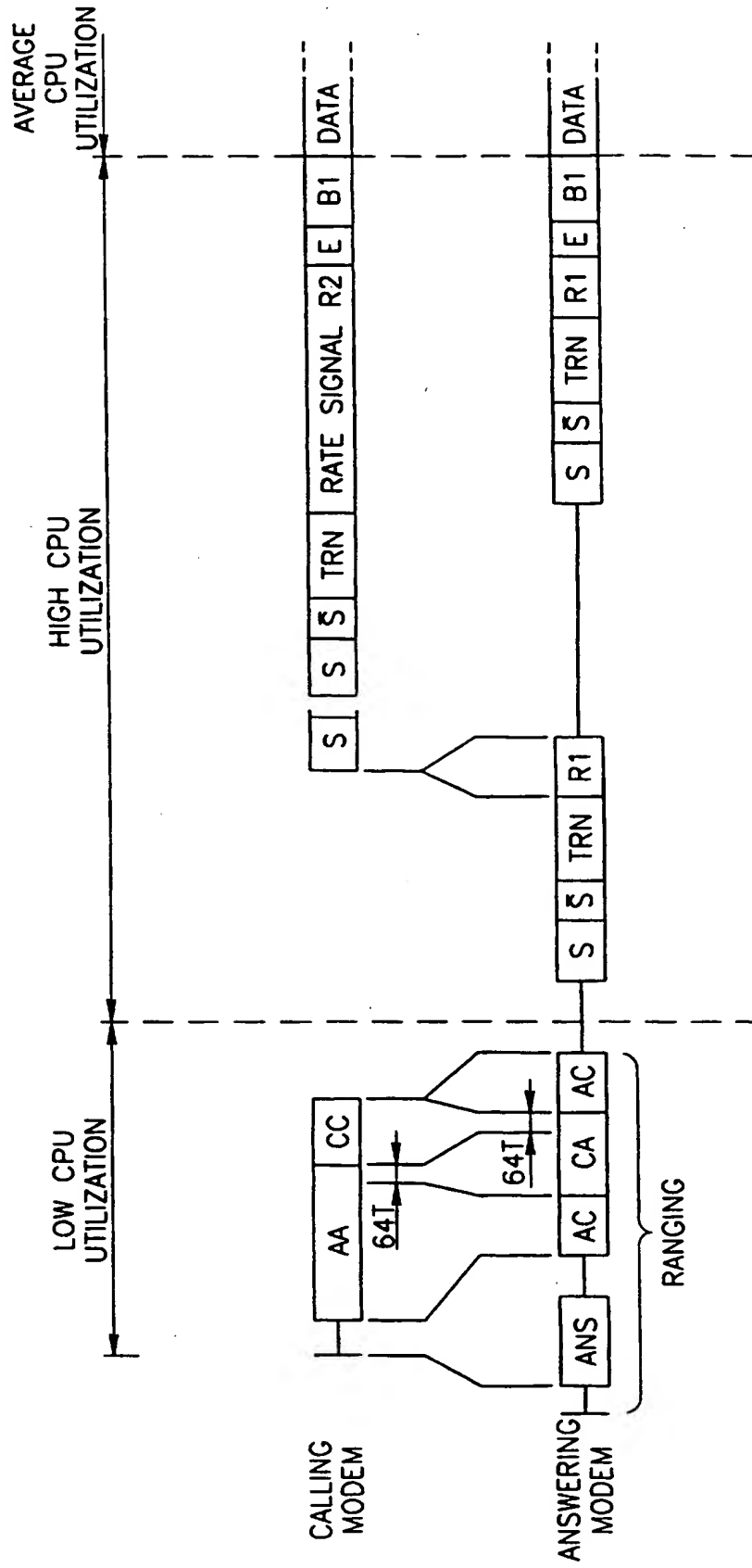


FIG. 4

FIG. 5 is a diagram illustrating a data flow and processing sequence over time. The diagram shows a sequence of samples (N-4, N-3, N-2, N-1, N, N+1, N+2, N+3) and corresponding processing steps (RECEIVE SAMPLES, PROCESSING, TRANSMIT SAMPLES). A decision point to switch is indicated between N-1 and N, leading to a switching point. Buffer sizes are specified as L1 and L2.

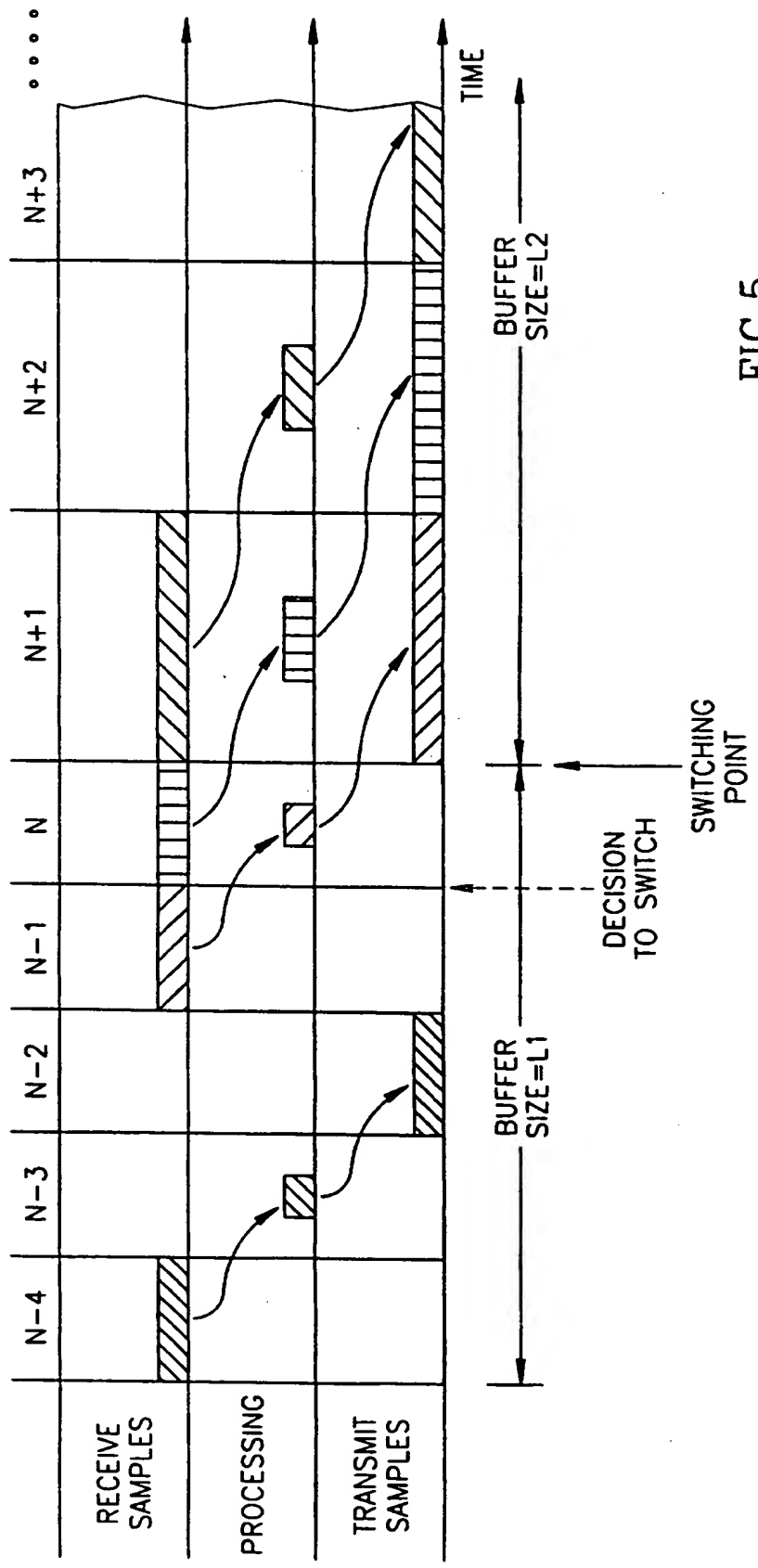


FIG. 5

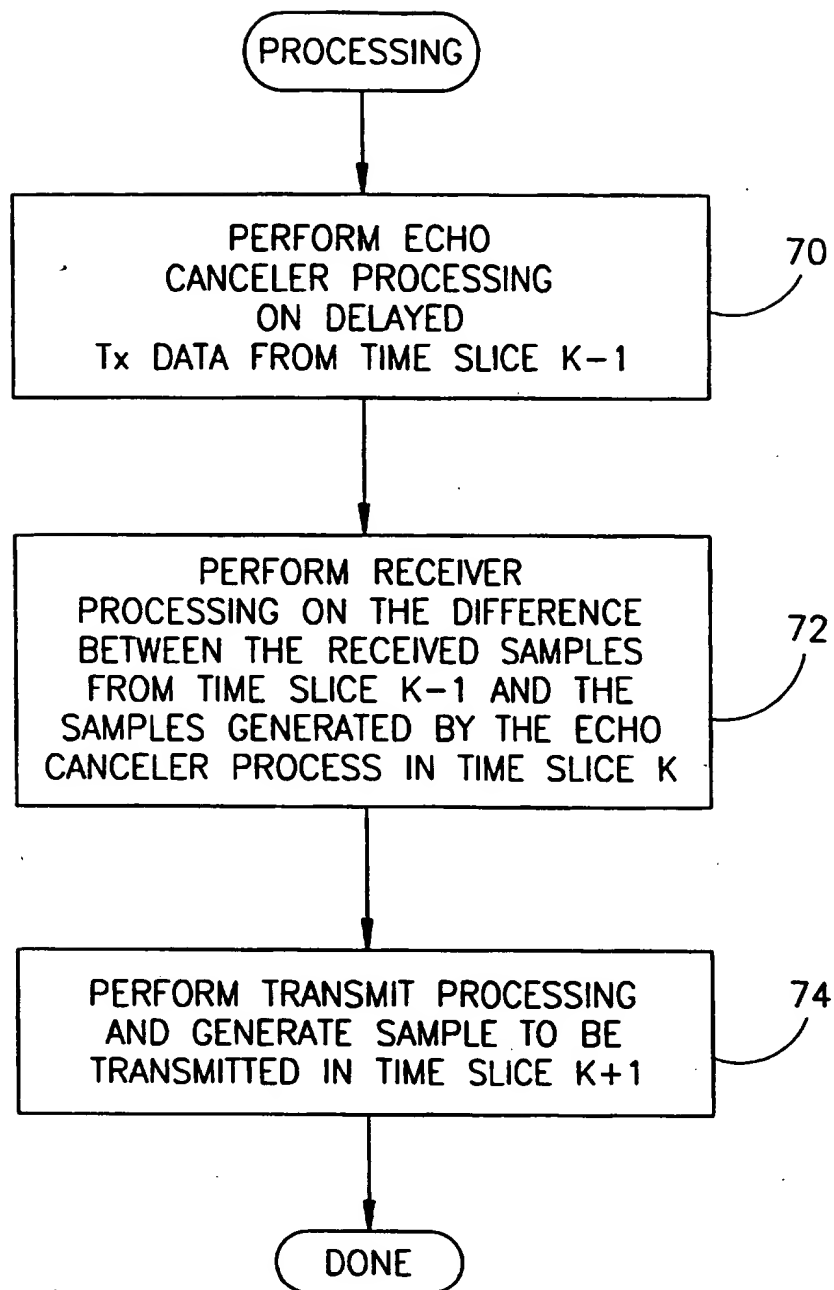


FIG.6